

U.S.S.N. 10,797,945

Specification Amendments

Please replace previously amended paragraph 0016 with the following re-written paragraph:

0016 Still referring to Figure 1A, the gate structures including gate dielectric portions may be formed by conventional CVD deposition, lithographic patterning, and plasma and/or wet etching methods known in the art. The gate dielectric may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, or chemical vapor deposition. [[s]]Silicon oxide, silicon nitride, silicon oxynitride, high-K (e.g., K > 8) dielectrics including transition metal oxides and rare earth oxides may be used for the gate dielectric.

Please replace paragraphs 0026 with the following re-written paragraph:

0026 Still referring to Figure 1E, a similar process as outlined for forming the first set of contact interconnects 30A, 30B, 30C, 30D, and 30E is then carried out to form a second set

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of contact interconnects e.g., 32A, 32B, and 32C extending through the thickness of the second ILD layer 22B to make contact (e.g., including overlying and at least partially encompassing) portions of the first set of contact interconnects. The second set of contact interconnects is formed according to the same preferred embodiments and aspect ratios as the first set of contact interconnects the first ILD layer 22A. **The second set of contact interconnects may have the same or different preferred aspect ratio as the second set of contact interconnects, for example having a smaller aspect ratio to ensure adequate interconnect overlap.** In addition, longer (horizontal to the substrate) contact interconnects e.g., 32A may be formed to conductively connect one or more of the first set of contact openings e.g., 30A and 30B. Preferably, the length of the longer contact interconnects, e.g., 32A is between about 0.15 microns and about 500 microns.